

Publications of Roberto Giorgi

Journal Papers and Book Chapters

1. S. BARTOLINI, I. BRANOVIC, R. GIORGI, E. MARTINELLI (2008). Effects of Instruction-set Extensions on an Embedded Processor: a Case Study on Elliptic Curve Cryptography over GF(2^m). IEEE TRANSACTIONS ON COMPUTERS, vol. 57; p. 672-685, ISSN: 0018-9340, doi: 10.1109/TC.2007.70832
2. S. BARTOLINI, R. GIORGI, E. MARTINELLI (2008). Instruction Set Extensions for Cryptographic Applications. In: C. K. KOC. Cryptographic Engineering. p. 191-233, BERLIN: Springer, ISBN/ISSN: 978-0-387-71816-3
3. S. BARTOLINI, P. BENNATI, R. GIORGI (2007). L'Informatica per i sordi: su palmare la lingua dei segni. MONDO DIGITALE, vol. 24; p. 42-49, ISSN: 1720-898X
4. R. GIORGI, N. PUZOVIC (2006). Scheduling and NoC Traffic Reduction in T-SDF Architecture. In: HiPEAC ACACES-2006. L'Aquila, July 26, GHENT: Academia Press, p. 253-256, ISBN/ISSN: 90-382-0981
5. R. GIORGI, Z. POPOVIC (2006). Core Design and Scalability of Tiled SDF Architecture. In: HiPEAC ACACES-2006. L'Aquila, Italy, July 26, GHENT: Academia Press, p. 145-148, ISBN/ISSN: 90-382-0981-9
6. S. BARTOLINI, P. FOGLIA, R. GIORGI, C. A. PRETE (2006). MEmory performance: DEaling with Applications, systems and architecture. COMPUTER ARCHITECTURE NEWS, vol. 43, No. 1; p. 1-2, ISSN: 0163-5964, doi: 10.1145/1152779.1147352
7. S. BARTOLINI, R. GIORGI (2006). Issues in Embedded Single-Chip Multicore Architectures. JOURNAL OF EMBEDDED COMPUTING, vol. 2, No. 2; p. 137-139, ISSN: 1740-4460
8. P. FOGLIA, R. GIORGI, C. A. PRETE (2005). Reducing coherence overhead and boosting performance of high-end SMP multiprocessors running a DSS workload. JOURNAL OF PARALLEL AND DISTRIBUTED COMPUTING, vol. 65, No. 3; p. 289-306, ISSN: 0743-7315, doi: 10.1016/j.jpdc.2004.10.003

Conference Papers

9. M. B. C. ALIOTO, P. BENNATI, R. GIORGI (2010). Exploiting Locality to Improve Leakage Reduction in Embedded Drowsy I-Caches at Same Area/Speed. In: IEEE Proceedings of the Int.l Symp. on Circuits and Systems. Paris, France, 30/5/2010-2/6/2010, NEW YORK: IEEE, vol. 1, p. 37-40, ISBN/ISSN: 978-1-4244-5309-2

10. R. GIORGI (2010) et al.. A Multi-Pronged Approach to Benchmark Characterization. In: IEEE Int.l Conf. on Cluster Computing. Heraklion, Greece, Sept. 2010, NEW YORK: IEEE, p. 1-4, ISBN/ISSN: 978-1-4244-8396-9, doi: 10.1109/CLUSTERWKSP.2010.5613090
11. R. GIORGI, S. WONG (a cura di) (2010). Proceedings of the 4th Workshop on Reconfigurable Computing. DELFT: TU-Delft / EWI Computer Engineering Laboratory, p. 1-116, ISBN: 978-90-72298-05-8
12. K. STAVROU, D. PAVLOU, M. NIKOLAIDES, P. PETRIDES, P. EVRIPIDOU, P. TRANCOSO, Z. POPOVIC, R. GIORGI (2009). Programming Abstractions and Toolchain for Dataflow Multithreading Architectures. In: IEEE Proc. Eighth Int.l Symp. on Parallel and Distributed Computing (ISPDC 2009). Lisbon, portugal, June 30-July 04, LOS ALAMITOS: IEEE, p. 107-114, ISBN/ISSN: 978-0-7695-3680-4, doi: 10.1109/ISPDC.2009.35
13. R. GIORGI, POPOVIC Z, PUZOVIC N (2009). Implementing hardware TLP support for the Cell processor. In: Proceedings of International Workshop on Multi-Core Computing Systems. Fukuoka, Japan, March 16-19, 2009, LOS ALAMITOS, CA: IEEE, p. 657-662, ISBN/ISSN: 978-1-59593-753-7, doi: 10.1109/CISIS.2009.177
14. R. GIORGI, Z. POPOVIC, N. PUZOVIC (2009). Exploiting DMA to enable non-blocking execution in Decoupled Threaded Architecture. In: Proc. IEEE Int.l Symp. on Parallel and Distributed Processing - MTAAP Multi-Threading Architectures and APplications. Roma, May, LOS ALAMITOS: IEEE, p. 1-8, ISBN/ISSN: 978-1-4244-3751-1, doi: 10.1109/IPDPS.2009.5161111
15. R. GIORGI, Z. POPOVIC, N. PUZOVIC (2009). Implementing Fine/Medium Grained TLP Support in a Many-Core Architecture. In: Proc. 9th Int.l Workshop on Embedded Computer Systems: Architectures, Modeling, and Simulation (SAMOS-2009). Samos, July, BERLIN: Springer, p. 78-87, ISBN/ISSN: 978-3-642-03137-3, doi: 10.1007/978-3-642-03138-0
16. S. BARTOLINI, P. FOGLIA, R. GIORGI, C. A. PRETE (a cura di) (2009). MEDEA '09: Proc. 2009 workshop on MEMory performance. NEW YORK: ACM, p. 1-48, ISBN: 978-1-60558-830-8
17. R. GIORGI, BENNATI P (2008). Filtering drowsy instruction cache to achieve better efficiency. In: Proceedings of the 23th ACM Symposium on Applied Computing. Fortaleza, Ceara, Brazil, March 11-15, 2008, NEW YORK: ACM, p. 1554-1555, ISBN/ISSN: 978-1-59593-753-7, doi: 10.1145/1363686.1364050
18. R. GIORGI, BENNATI P (2008). Reducing Leakage through Filter Cache. In: Proceedings of the 11th EUROMICRO-DSD. Parma, Italy, September 3-5, 2008, LOS ALAMITOS, CA: IEEE, p. 334-341, ISBN/ISSN: 978-0-7695-3277-6, doi: 10.1109/DSD.2008.123
19. R. GIORGI, Z. POPOVIC, N. PUZOVIC, A. AZEVEDO, B. JUURLINK (2008). Analyzing Scalability of Deblocking Filter of H.264 via TLP

Exploitation in a New Many-Core Architecture. In: Proceedings of the 11th EUROMICRO-DSD. Parma, Italy, September 3-5, 2008, LOS ALAMITOS, CA: IEEE, p. 189-194, ISBN/ISSN: 978-0-7695-3277-6, doi: 10.1109/DSD.2008.93

20. S. BARTOLINI, P. FOGLIA, R. GIORGI, C. A. PRETE (a cura di) (2008). MEDEA '08: Proc. 2008 workshop on MEMory performance. NEW YORK: ACM, p. 1-84, ISBN: 978-1-60558-243-6
21. R. GIORGI, P. BENNATI (2007). Reducing leakage in power-saving capable caches for embedded systems by using a filter cache. In: Proceedings of the MEDEA 2007 Worskhop on Memory Performance: Dealing with Applications, Systems and. Brasov, Romania, September 17, p. 105-112, ISBN/ISSN: 978-1-59593-807-7
22. R. GIORGI, Z. POPOVIC, N. PUZOVIC (2007). DTA-C: A Decoupled Threaded Architecture for CMP Systems. In: Proc. of IEEE SBAC-PAD. Gramado, Brasil, October 24, p. 263-270, ISBN/ISSN: 0-7695-23014-1
23. S. BARTOLINI, P. FOGLIA, R. GIORGI, C. A. PRETE (a cura di) (2007). MEDEA '07: Proc. 2007 workshop on MEMory performance. NEW YORK: ACM, p. 1-113, ISBN: 978-1-9593-807-7
24. S. BARTOLINI, P. FOGLIA, R. GIORGI, C. A. PRETE (a cura di) (2006). Proceedings of the 2006 workshop on MEMory performance: DEaling with Applications, systems and architectures. Di VARI., NEW YORK, NY: ACM Press, p. 1-52, ISBN: 1-59593-568-1